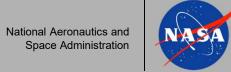
Japan Aerospace Exploration Agency (JAXA) The 30th Microelectronic Workshop (MEWS30) October 18-19, 2017



NASA Electronic Parts Activities: Ongoing and Recent Initiatives



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- Thank you Shindou-san for your invitation. It's always a great pleasure to visit Tsukuba.
- Congratulations on the 31st anniversary of the MEWS Workshop!
- Even more so, congratulations to JAXA on Hayabusa 2 landing on the asteroid 162173 Ryugu.
- JAXA is our valued partner in NASA Electronic Parts Assurance Group (NEPAG) activities.



Introduction



- This talk is about NASA's parts activities.
- We'll review the ongoing activities and the recent initiatives including Electronic Parts and ElectroStatic Discharge (ESD).
- This is NASA's 60th anniversary. A lot has happened during this period. Many notable successes kept us going. The failures gave an opportunity to make process improvements.
- Thru this all, the mission assurance organizations at NASA have supported many space missions/programs, large and small. Today, that spectrum has grown wider, ranging from smallsats/cubesats to flagship missions such as the planned Europa mission. As always, the success of each and every mission counts.
- The nature of our business warrants that we strive for lower power, higher performance, more functionality, and smaller packages.
- The missions today are global in nature with many joint efforts with our international partners. As NEPAG, we work with manufacturers and the space parts user community to develop/evaluate new space products.
- The following pages will discuss some of the recent activities and challenges.
- We'll end the talk with a couple of short videos.

Partnering



JEDEC JC-13 (Manufacturers)

JC-13	Solid State Devices for Government Products
JC-13.1	Discrete Semiconductors for Government Products
JC-13.2	Microelectronics for Government Products
JC-13.4	Radiation Hardness
JC-13.5	Hybrids and Multi-chip Modules for Government Products
JC-13.7	New Electronic Device Insertion for Government Products

Joint meetings held 3 times a year



SAE CE-11/CE-12 (Industry Users, Primes, Subs)

SAE SSTC CE-11	Users of Passive Components
SAE SSTC	Users of Solid State Devices
CE-12	CE-12 Management:
	Chair – A. Touw Vice Chair – (JPL) S. Agarwal
SAE SSTC CE-11 & CE-12	Space Subcommittee Chair – S. Agarwal

NASA Centers:

ARC JSC
GRC KSC
GSFC LaRC
JPL MSFC

Weekly Telecons (Domestic)

Monthly Telecons (International)

Partners from Outside NASA:

Domestic JHU/APL, Others The Aerospace Corp, U.S. Air Force, U.S. Navy, U.S. Army, DLA,

International ESA, JAXA, CSA

NASA and JC-13



- NASA is an active participant in many JC-13 activities.
- Some of the JC-13 Task Groups were started at NASA's request.
 - Example: Electronic Parameters and Burn-in Standardization.
- The newly started New Technology initiative (JC-13.7) provides a look ahead
 - Identify new technologies, develop path for their infusion into military & space
 - A task group (TG) on Organic Substrate Class Y was started in September'18.



JAXA's Hayabusa 2 landed on the asteroid 162173 Ryugu on September 21, 2018 and began taking data.

NASA's JPL Deep Space Network (DSN) has a modest role of supplying a communications link with the probe. Shown to the left are antennas in the Canberra Deep Space Complex of the DSN.

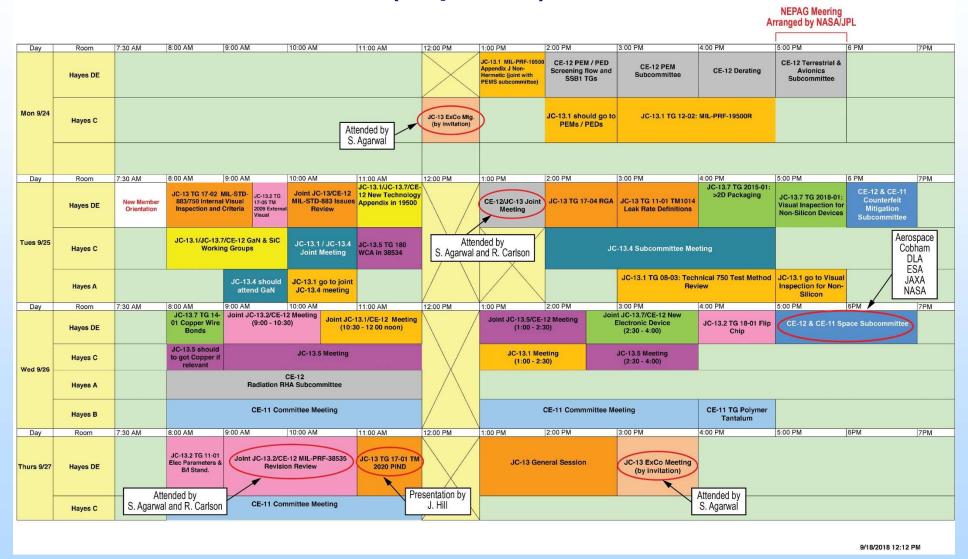
NASA and SAE SSTC CE-12*



- NASA is an active participant in many CE-12 activities.
- When requested, NASA has led the CE-12 Task Groups.
 - Example: Infusion of new technology into DoD standards, the Class Y initiative.
- With the appointment of Shri Agarwal as the Vice-Chair of CE-12, NASA is helping run the organization.
- NASA was asked to take over the CE-12 Space subcommittee as its Chair. In addition to the regular presentations from international agencies and United States organizations, the following presentations were made at the September 26, 2018 meeting: State of Space Grade Crystal Oscillators, Data Retention, and update on NEPP/Cobham joint effort on organic class Y.
- * SAE = Society of Automotive Engineers
 SSTC = Systems, Standards and Technology Council
 CE-12 = Solid State Devices

Meeting Schedule for JEDEC JC-13/CE-11/CE-12 (Sep 2018)





New Technology Evaluation A Multi-pronged Effort



- New Technology Evaluations
 - There are NEPP (NASA Electronic Parts and Packaging) funded evaluations
- The JC-13 Effort
 - A few years back, JC-13 created a new committee, JC-13.7
 - **❖** JC-13.7 charter is to look into next generation technologies
 - List of top candidates
 - Organic Substrate Class Y
 - ✓ A new task group started (Sept 2018)
 - √ This would expand into 2.5D and 3D configurations
 - Others:
 - ✓ SiC, GaN Added ESD to the scope
 - ✓ Copper wire bonds
 - What would it take to infuse new technologies into QML standards
 - Identify the gaps
 - The effort is supported by NASA, JAXA, ESA among others

New Technology Evaluation A Multi-pronged Effort (Cont.)



- Preparing to embrace advanced technologies
 - Continually Improving the Existing Infrastructure
 - The role of Microcircuits Qualifying Activity (QA)
 - QML Classes
 - > Is the current set of Q, V, and Y sufficient to cover new devices?
 - Specifications and Standards
 - Bring them current (more details later)
 - Some of the side issues
 - Handling/packaging/ESD (electrostatic discharge)
 - Burn-in of high speed devices
 - Usefulness of the Qualified Products List (QPL) program
 - QPLS (space grade) crystal oscillators Limited resources
 - √ No one buying them
 - ✓ DLA effort underway to update the general specification (NASA is supporting)

New Technology - Some Major Activities



- Technical support to the Defense Logistics Agency (DLA) audits of supply chain:
 - Wafer foundry
 - Wafer bumping
 - Assembly and test: added one more supplier for Class Y (already approved for Q and V)
 - Column attach: added one more supplier for Classes Q, V, and Y
 - Proper shipping/handling/ESD precautions become important
 - Per unit costs approaching \$200k
 - NASA ESD surveys
 - Performed 10 ESD surveys
 - > Published three special issues for NASA EEE Parts Bulletins
- Qualifying Activity (QA) Reviews/Approvals:
 - NASA is part of the QA
 - Manufacturers to perform qualification as required in MIL-PRF-38535.
 - ❖ For example, a 4000-hour life test
 - DLA and manufacturers to develop standard microcircuit drawing (SMD)
 - Update existing boiler plate to accommodate new features example on next page

An Example of SMD Boiler Plate Update



TABLE IIA. Electrical test requirements.

Line Number	Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
Number		Device class Q	Device class V
1	Interim electrical parameters (see 4.2)	1,2,3,7,8A, 8B,9,10,11 <u>1</u> /	1,2,3,7,8A, 8B,9,10,11 <u>1</u> /
2	Static burn-in I and II (method 1015)	Not required	Required
3	Same as line 1		1, 7 Δ <u>1</u> / <u>2</u> /
4	Dynamic burn-in (method 1015)	Required	Required
5	Same as line 1	1,7 Δ <u>1</u> / <u>2</u> /	1, 7 <u>∆</u> <u>1</u> / <u>2</u> /
6	Final electrical parameters	1,2,3,7,8A,8B,9, 10,11 <u>1</u> /	1,2,3,7,8A,8B,9, 10,11 <u>1</u> /
7	Group A test requirements 3/	1,2,3,4,7,8A,8B,9,10 ,11 <u>4</u> /	1,2,3,4,7,8A,8B,9, 10,11 <u>4</u> /
8	Group C end-point electrical parameters 3/	1,2,3,7,8A,8B, 9,10,11 <u>\(\(\(\) \) 2</u> /	1,2,3,7,8A,8B, 9,10,11 ∆ <u>2</u> /
9	Group D end-point electrical parameters 5/	2,3,8A,8B	2,3,8A,8B
10	Group E end-point electrical parameters <u>3</u> /	1,7,9	1,7,9
11	Column attach <u>6</u> /	1,7,9	1,7,9

For Flip-chip column attach

 Add room temperature electricals (subgroups 1, 7, 9) after column attach – step 11 above

NASA's Involvement in Developing New Space Products



- With the Defense Logistics Agency (DLA) and the Aerospace Corporation, NASA participates in the review and approval of new space products:
 - Standard Microcircuit Drawings (SMDs)
 - Characterization and qualification data per Appendix H of MIL-PRF-38535 (for the monolithics)
- During fiscal year 2018, 16 microcircuit SMDs were approved for release. The mix of new product types included:
 - Rad hard reprogrammable field-programmable gate arrays (FPGAs) from Atmel/Microchip Technology
 - High-speed Analog-to-digital converters from Texas Instruments (TI)
 - Rad hard DC/DC converters from International Rectifier
 - Rad hard and non rad hard DC/DC converters from VPT Inc. (VPT)
 - Operational amplifiers from Analog Devices, Inc. (ADI)
 - Rad tolerant FPGA from Microsemi/Microchip Technology
 - And others
- □ Per manufacturers, there is a continuing strong demand for space products

Example of Updated Requirements, Microcircuits Burn-in (BI) (NASA Inputs 12 September 2016)



Status

- Task Group (TG) chaired by N. Shindler
- Published Guideline document JEP163.
- Task Group is still open to address new concerns.
- The last TG meeting decided to produce a white paper on the on-going concerns (see below)

On-going Concerns

- Ambient vs. case vs. junction temperature
- Bl of high-speed devices (frequencies approaching gigahertz range)
 - What about hot spots on the die? For example, a serializer/deserializer (SERDES) in an FPGA may run much hotter than the rest of the die.
 - Practically no data on hot spots (no verification of models)

JEDEC PUBLICATION

Selection of Burn-In/Life Test Conditions and Critical Parameters for QML Microcircuits

JEP163

SEPTEMBER 2015

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



The "Class Y" Initiatives



- It was recognized by the community that packaging and device technology advances are happening rapidly.
- In order to enable space flight projects to benefit from the newly developed devices, e.g., Xilinx Virtex-4 and -5 FPGAs (which are ceramic-based flip-chip nonhermetic parts), a new class was needed.
- NASA led a CE-12 initiative, called Class Y, for infusing Xilinx FPGAs and other similar devices into military/space standards.
 - Such an effort must be coordinated with the suppliers and users.
 - Need to address all aspects of packaging configuration.
 - New test methods must be created and the existing standards updated as necessary.
- A Follow-on to Ceramic Substrate Class Y
 - The JC-13.7 task group created a new task group on organic substrate Class Y at the September 2018 meeting.

Infusion of New Technology into MIL/Space Standards PIDTP and Its Applicability



Issue

 How to address the manufacturability, test, quality, and reliability issues unique to new non-traditional assembly/package technologies intended for space applications

Solution implemented

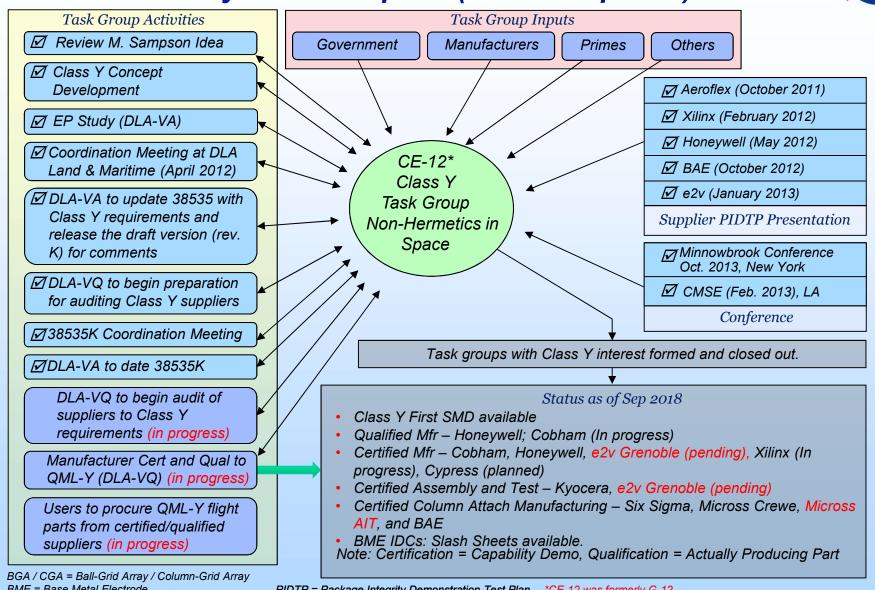
- A new concept: package integrity demonstration test plan (PIDTP)
- Each manufacturer shall develop a PIDTP to be approved by the qualifying activity after consultation with the space community.

The PIDTP requirement applies to:

- Non-hermetic packages
- Flip-chip assembly
- Solder terminations
- o (Refer to 38535, Appendix H)
- The PIDTP approach seems to be working well so far.

Infusion of the Class (Y) Technology into the QML System for Space (Status Sep2018)





BME = Base Metal Electrode IDC = Inter Digitized Capacitor

PIDTP = Package Integrity Demonstration Test Plan *CE-12 was formerly G-12

QML = Qualified Manufacturers Listing SMD = Standard Microcircuit Drawing

Electronic Parts and Electrostatic Discharge (ESD) – Gaps and Mitigation Strategies



- Gaps have evolved because of new technology and inconsistencies of standards development (e.g., three zaps vs. one zap per pin for testing). Parts have continued shrinking to smaller sizes & growing in complexity. Consequently, they are more susceptible to ESD and require more testing effort.
- Costs cannot be ignored—per unit price for advanced devices is approaching \$200K. ESD mitigation costs are minute compared to the device unit costs.
- Mitigation strategies include ESD surveys, observations during audits, standards updates (including harmonization of standards), & outreach to the military & space communities.

Why Electronic Parts and ESD Need a Fresher Look--Gaps



- NASA has been supporting Defense Logistics Agency (DLA) audits of the supply chain.
- During the audits, it was observed that the MIL-PRF-38535 requirements were practically nonexistent regarding ESD aspects of electronic parts.
- Microcircuit pin count has increased significantly (e.g., Vertex FPGAs have 1752 columns). Manufacturers are striving for still higher counts.
- Current qualification standards were developed years ago with pin counts in the twenties.
- Applying these old device testing standards to modern high-pin count products can cause severe problems (e.g., testing times increase dramatically).
- Furthermore, microcircuit part production is no longer under one roof, but landscape of supply chain is multiple specialty houses (see next slide).

Need to update standards

A Changing Landscape (Shipping/Handling/ESD Challenge)

A New Trend – Supply Chain Management Ensuring gap-free alignment for each qualified product (All entities in the supply chain must be certified/approved)

Manufacturer A	Die design
Manufacturer B	Fabrication
Manufacturer C	Wafer bumping
Manufacturer D	Package design and package manufacturing
Manufacturer E	Assembly
Manufacturer F	Column attach and solderability
Manufacturer G	Screening, electrical and package tests
Manufacturer H	Radiation testing

More Stops — More Places with ESD Risk

Electronic Parts and ESD – NASA Concerns



- MIL-STD-883, Test Method 3015
 - Too old
 - Does not include the charge device model (CDM), only the human body model (HBM)
 - The Test Method needs to be revisited for new technology
 - Smaller feature sizes (down to 30 nm)
 - **❖** Large number of contacts/pins (e.g.,~1750 for Xilinx FPGA)
 - Vastly increased time to test
 - Advancements in packaging (2.5D, 3D)
- MIL-PRF-38535 Performance specification for microcircuits
 - DLA audits of microcircuit manufacturers and their supply chains
 - ❖ Are done to the requirements stated in 38535
 - 38535 is at revision K. Draft L revision is being worked.
 - Poor coverage for ESD
 - No CDM testing required
 - Confusing requirements
 - > 883 vs. JEDEC (3 zaps/pin vs. 1 zap/pin, for HBM test)
 - **❖** No requirements for wafer foundries
 - Needs to be updated
 - For new technology
 - For shipping and handling of products in multi-supply chain production of parts (which is becoming the norm)

Activities to Improve ESD and Electronic Parts



- Continuing NASA ESD Surveys
 - Conducted by NASA experts
- Added requirement in 38535K for post column attach electricals
 - To catch handling/ESD related problems
- JC-13 Started a Task Group on ESD (Chair: P. Coe of Cobham, Colorado Springs, CO)
 - The fact that it is a JC-13 task group means that it has the highest level of attention and applies to all commodities
 - The task group is already active
- JEDEC/ESDA Are Continuing Joint Effort
 - JESD 625B and ESDA S20.20 Harmonization telecons and face-to-face meetings
 - Participation by NASA and Aerospace Corporation

NASA ESD Surveys of Microcircuit Supply Chain



NASA ESD Surveys

- Benefits not only NASA but the whole community
 - Especially vendors processing very expensive new technology parts (per unit price could approach \$200k)
- Candidate companies are identified during DLA audits—but not a DLA activity
- Conducted by NASA ESD experts
 - The survey findings and corrective actions have been merely suggestions for improvements (but, in all cases, were implemented by the vendors)
- Very well received
 - Vendors have implemented most suggestions
 - Some vendors have requested re-surveys every two years
- Working with Suppliers and DLA to incorporate NASA ESD Surveys into DLA audit agendas
 - Make efficient use of resources
 - Was done two times and worked well

Example ESD Survey Findings



Chairs

- In several cases, chairs were noted to be non-ESD Safe
 - ❖ Remove/relocate/replace non-ESD chairs
- One chair repaired with non-Safe tape

Ionizers

- In limited use.
- Certified every 12 months. JPL 34906 requires 6-month intervals.
 S20.20 allows it to be at the supplier discretion.

Tape

Dispensed where no air ionizer was available

CRT Monitors

These are charge generators. Found near parts in engineering test.
 CRT displays are not recommended.

Wrist Straps

Cloth wrist straps were used typically. Prohibited per JPL 34906.

ESD Outreach by NASA



NASA Is Highlighting ESD in EEE Parts Bulletins

- Released three special editions on ESD. The first dealt with the need to upgrade specifications related to ESD and suggestions for better ESD practices wherever parts are manufactured, stored, or prepared for shipment.
- The second ESD special issue focused on a parts failure investigation that ultimately concluded that ESD was the most likely cause of the failure. The second issue also included an important reminder about regular ESD testing.
- A third issue provided an example demonstrating the importance of maintaining ESD discipline and a high-level risk analysis related to electrostatic discharge.

Invited ESD Talks

- Special JEDEC JC-13 talk by ON Semi, Manila, Philippines (scheduled Jan 2019)
- Micross/STS at CE-12 Space Subcommittee in 2016 chaired by NASA

Electrostatic Discharge



NASA EEE Parts Bulletin (August 2016 – May 2017)



August 2016–May 2017 • Volume 9, Issue 1 (Published since 2009), June 16, 2017

Second Special Edition on Electrostatic Discharge (ESD)

Damage from ESD is a major cost to the microcircuit industry in terms of time, money, and mission risk. The first issue dealt with the need to upgrade specifications related to ESD and suggestions for better ESD practices wherever parts are manufactured, stored, or prepared for shipment. This second ESD special issue focuses on a parts failure investigation that ultimately concluded that ESD was the most likely cause of the failure. The issue also includes an important reminder about regular ESD testing and a table of standard microcircuit drawings that were recently reviewed.

Figure 1 is an example of damage that was probably caused by ESD.



Fig. 1. Detailed view of a damaged site on a metal oxide semiconductor field-effect transistor (MOSFET) probably caused by FSP.

ESD, the Silent Killer-

A. Background

There are several great points to consider with respect to ESD knowledge, practice, and compliance. However, the key for ESD program success is consistency. If we detect the results of an event, then, we [the operational group] should be able to ascertain and confirm that we never have any lapses in the program implementation. With systematic practices, we should be able to surmise that there

is no way any events can occur on the organizational project watch.

ESD is the silent killer in electronics, and the resulting impacts are hidden project costs that are the motivator to address project risk cost and schedule impacts. When an ESD event occurs, one of three scenarios may play out.

- 1) There is no impact, and no detrimental result.
- 2) There is a catastrophic strike and the immediate

h failure is detected, isolated, irs may be easy or done at hey are done.

le event may happen. Undene or more parts results in laare either detected during ns or (worse yet) during misen any resulting failures may

pens in the product life cycle he project cost for repair, Lation is weak due to lack of acmalfunctioning hardware for

we need the highest possible D program compliance at all ctive.

nnly include part costs, which (for a typical active part) to rrogrammable gate arrays, labor and mission assurance real hidden costs can potening the diligence to complete failure analysis, possibly nuview boards and completion disposition of the ESD failure

alone associated with all the uthorities, subject matter exare assembly personnel attings can in most cases out of the damaged part alone, so participate in system tearpart screening/testing of the new part, reassembly, and em. Therefore, prevention is

nedule impacts. When an scenarios may play out. strike and the immediate strike strike and the immediate strike s

and shipped off for failure analysis.

Figure 2 shows the PCB assembly with two noted nonfunctional parts circled in red. Although not conclusive, the corner location of damaged parts on the board was thought to be important to the forensics analysis. One theory implied that handling of the board (by the perimeter) allowed for the ESD event to contact these parts directly. During transport, the board is handled only inside an ESD-approved materials bag. There were questions as to the integrity of these transport bags. Due to bag fraceability and reuse issues, there was no definite conclusion on this concern.

Figures 3 thru Figure 7 Show the die and damage areas from various photographic and radiographic perspectives. During upper-level assembly circuit troubleshooting, the potential for design or operational damaging voltages to the MOSFET gates were conclusively ruled out. The circuit was incapable of generating the necessary damaging voltages that would have the effect observed.



The conclusion of this ESD failure investigation was that failure was attributed to user error but review of all ESD compliance logs showed that all precautions were taken during operator handling. Due to lack of further evidence, the OCM and the PCB assembly operation were not ruled out as possible culprits, but neither could be confirmed.

Under these circumstances the team was advised of the event and warned of the total cost for repair and the need to double check all future handling procedures. The board was repaired with same lot date code parts, and there were never any repeat operational issues with that PCB assembly nor at the box operational level. The "Silent Killer" only struck once on that program. At least as far as can be determined at this time.

Figures 1 through 7 (provided courtesy of NASA Langley Research Center) were generated by Hi-Rel Labs as part of a project Component Failure Investigation at Langley.

For more information, contact John E. Pandolf 757 864-9624



circled in red.



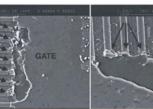
Fig. 3. Optical micrograph of the die in the failed device. The red arrows indicate the damage sites.



mane sites on the die



Fig. 5. SEM image of one of the damage sites. The arrow indicates the area where the damage originated



ET after delayering. The arrows in icate the damage at the ends of the gate runners.

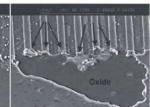
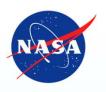


Fig. 7. SEM image of another damaged area on the die. Note that the gate polysilicon fused during the failure, which is why the oxide is visible.

3

2

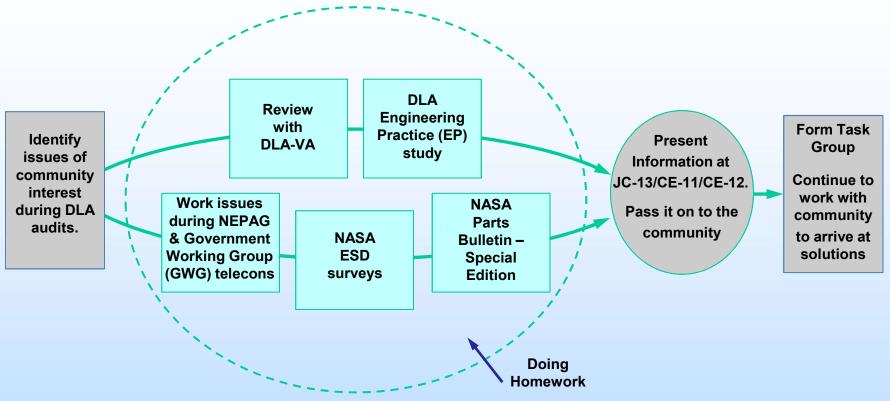
NASA Inputs to JC-13 ESD TG Meeting Jan. 25, 2018



- MIL-PRF-38535 Rev L (Draft)
 - Available on DLA website. Has several updates on ESD. NASA will review and provide comments
 - Want to make sure some of the items we brought up before are not forgotten
 - **❖** No specific requirements for wafer foundries
 - Suggested solution: Replace "Devices" with "Wafers/Dice/Devices" such as in Para A.4.4.2.8:
 - A.4.4.2.8 Electrostatic discharge (ESD) sensitivity.
 Wafers/dice/devices shall be handled in accordance with the manufacturer's in-house control documentation, which shall be maintained by the manufacturer......
 - Add requirements for shipping and handling of products in multisupply chain production of parts (which is becoming the norm).
 - * (New) Look into ESD behavior of high-speed pins
- MIL-STD-883, Test Method 3015
 - MIL-PRF-38535 Rev L calls out JS-001 as an alternate to 3015. Should compare the two and identify differences.

Taking Audit Findings a Step Further! NASA Timesaving Approach





- Bring general awareness (Via NASA Bulletins, Surveys)
- Work with DLA to help them conduct an engineering practice (EP) study
- Generate a basic proposal and related information so the potential task group (TG) has a strong starting point.
- This path has saved time in resolving major issues found during audits.

Growing Use of NASA Cubesats and Smallsats



- Trend toward cubesats and smallsats
 - Many new NASA flight missions are cubesats and smallsats.
 - The weekly NEPAG telecons discuss types of standard products that would fit those applications, including commercial-off-the-shelf (COTS) plastic encapsulated microcircuits (PEMs).
- The parts manufacturers are offering customized parts, e.g.,
 - Cobham Aeroflex has several flows assigned based on extent of testing to assist users in picking the best parts.
 - Texas Instruments offers parts in five different versions, including their QML offerings.
 - Linear Technology (now a part of Analog Devices, Inc., ADI) plans to offer PEM products with guaranteed total dose radiation (rad tolerant, RT) ratings.

Standardized Flows for NASA Cubesats and Smallsats



The need for standardization

- The developments discussed on previous slide are all good, but
- It would be cumbersome to manage multiple nonstandard flows.
- Moreover, some of these approaches may or may not apply to NASA missions depending on acceptable risk levels.

Possible methods to get standardized flows

- The ideal situation would be for the space community and manufacturers to agree on a limited number of standard QML PEM flows to offer solutions for small missions (cubesats, nanosats, smallsats, etc.).
- There is an existing QML N flow for standard non-space PEM devices.
- CE-12 developed a document SAE AS6294. That would be a good starting point.
- In addition, DLA has the Vendor Item Drawing (VID) program and parts built for automotive applications.

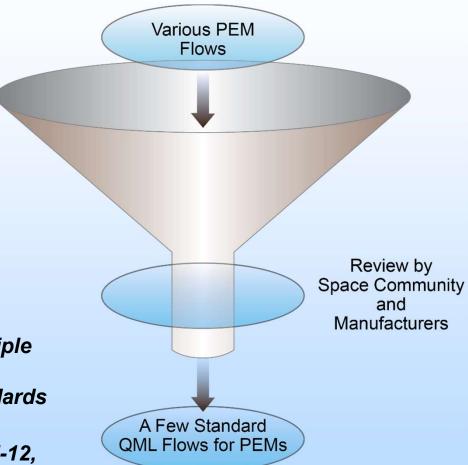
PEMs for Space



- Newer Applications
 - Cubesats
 - Smallsats

Standardizing on a few welldefined flows rather than multiple flows defined by each manufacturer or by each standards group.

SAE AS6294, developed by CE-12, would be a good starting point.



Evaluating Automotive Parts for Potential NASA Applications



- The main drivers are size, weight, and price of electronic components
 - Commercial electronic parts usually offer varied functions
 - How do automotive parts compare to catalog commercial?

Commercial Parts Options

- Manufacturers make parts to meet the needs of their chosen market(s)
- Automotive parts are designed to meet the needs of subsystem suppliers to automobile manufacturers

Space

- Parts from manufacturers that are qualified to the Automotive Electronics Council (AEC) Q specifications seem to offer advantages for the smallsat users
- NASA is doing a limited evaluation of automotive electronic parts

Counterfeit Parts



- Refers to counterfeit parts awareness and mitigation.
- GIDEPs (Government Industry Data Exchange Program [reports])
 on counterfeit parts are reviewed on NEPAG telecons. They are
 trending downwards.
- During the DLA audits, the manufacturers are asked for their counterfeit mitigation plans. Most manufacturers have some form of mitigation.
- NASA provides counterfeit training.
- NASA supports the SAE (Society of Automotive Engineers) counterfeit mitigation effort.
- Procure parts, particularly new technology devices, from the authorized sources.

NASA's Electronics Technology Workshop (ETW)



- The ETW is held in June every year
- Venue: Goddard Space Flight Center, Greenbelt, MD
- Past papers posted on NEPP Website: nepp.nasa.gov
- See above website for other details
- ETW 2019 will be held June 17–20, 2019

Conclusion



- Incorporating new technology into our hardware is an on-going challenge.
- NASA brought many ESD concerns to the attention of the parts community.
 - Affects all commodities for both military and commercial parts
 - COTS hardware could be affected more severely
 - Parts community must promote an ESD-safe environment!
 - Be mindful of ESD when shipping / handling parts and hardware!
- NASA is working with the space community to help infuse new technologies during the coming decade – including organic Class Y and molded plastic parts.
- The JAXA Microelectronics Workshop (MEWS) is an extremely useful resource in these endeavors.

Thank you!

http://nepp.nasa.gov



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Government sponsorship acknowledged.